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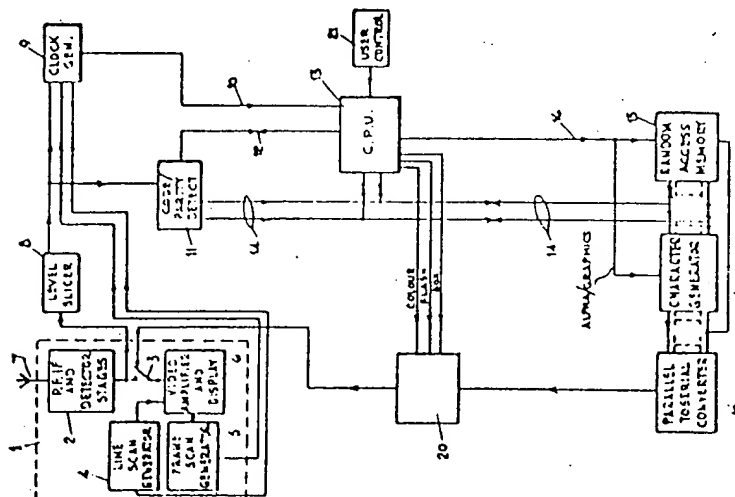
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Data receiver on TV channel during line scans not in use - has memory with character generator, central processing unit and parallel-to-serial converter

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TV receiving appts. is adapted for the display of information characterising data which is transmitted during line



PATENT SPECIFICATION

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(19)



(54) IMPROVEMENTS IN OR RELATING TO RECEIVING APPARATUS FOR COMBINED TELEVISION/DATA DISPLAY SYSTEMS

(71) We, THE ENGLISH ELECTRIC COMPANY LIMITED, of 1 Stanhope Gate, London W1A 1EH, a British Company, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:-

The present invention relates to receiving apparatus for a combined television/data display system and more particularly to receiving apparatus designed to receive information characterising data to be displayed transmitted during line scan periods of a television signal when picture information is not being transmitted.

The receiving apparatus is included as part of a television set and the normal picture displayed on the television screen may be replaced by the decoded information. For the purposes of the present invention such decoded information will be referred to as data and the normal television picture information will be referred to as the picture.

With one known type of transmission system for the data the information which is transmitted consists of a number of "pages", each page of data representing a complete television display. Each page may for example be of the form of 24 rows with 40 characters per row and each page commences with a special top row called the Page Header. The pages are each numbered and a group of for example 100 pages forms a magazine. A number of magazines are provided and the viewer can select which page of which magazine is required by means for example of selection switches.

The viewer requires to be able to select a desired page for viewing and the apparatus is required to detect the transmission of the particular page, to store the page and subsequently to provide the necessary signals to display the desired page.

In known apparatus, for example in United Kingdom Patent No. 1,467,240, the apparatus has been constructed from electronic blocks which each perform a specific function. It is an object of the present invention to perform one or more of these functions in a Central Processing Unit (C.P.U.) and thereby simplify the circuitry of the known apparatus.

According to the present invention there is provided apparatus for a combined television/data display system in which information characterising data to be displayed is transmitted during line scan periods of a television signal when picture information is not being transmitted, comprising a memory for the storage of said information, character generator means for generating electric signals in respect of data characters to be displayed, and a central processing unit operable under the control of a program for controlling the storage of said information and the operation of said character generator means.

An advantage of the arrangement according to the present invention is that by alteration of the program a number of different functions may be obtained. For example the television display may be used to display information received not from a television transmission but fed in from a data modem, from an attached key board, a magnetic tape unit or other source of data.

In general however for any particular application the computer program will be stored in a read only memory and the apparatus will perform only a specific function.

Embodiments of the present invention will now be described, by way of example, with reference to the drawings accompanying the provisional specification, in which:-

Figure 1 shows in block diagrammatic form one possible television display and receiving apparatus, and

50 CPU
improvement

70 Software

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Figure 2 shows the central processing unit of Figure 1 in more detail.

Referring now to Figure 1, a television/data receiver 1 is shown within dotted lines. The receiver comprises RF and IF detector stages 2, a switch 3 for changing the display from the normal television picture to the display of data, a line scan generator 4 and a frame scan generator 5 which control a video amplifier and display unit 6.

Television transmission signals are received at an aerial 7, detected by detector 2 and fed either both to the video amplifier and display 6 and a level slicer 8 or, when the set is displaying data, only to the level slicer 8. The output of level slicer 8 is fed to a clock generator circuit 9 together with outputs from the line and frame scan generators 4 and 5. Clock generator 9 produces clock signals to synchronise the rest of apparatus not yet described via line 10.

The output of the level slicer 8 is fed to a code and parity detect circuit 11 which detects start codes and ensures that the parity of information is correct. An output 12 of the code and parity detect circuit is fed to a Central Processor Unit 13 to provide the C.P.U. with information relating to the input data. The input data is fed on data bus 14 to inputs of the C.P.U. and to a random access memory 15 into which it is fed under the control of the C.P.U. obtained via line 16. The output of the random access memory 15 is able to be fed back to the C.P.U. 13 on data bus 14 and via character generator circuit 18 and parallel to serial converter circuit 19. The output of the parallel-serial converter 19 is fed via a control box 20 to the video amplifier and display circuit 6 via the switch 3. Control box 20 has inputs from the C.P.U. 13 to control the colour of the data to be displayed, to control the flashing on and off of certain characters and to control the production of a "box" for display, in an overlay manner, of data superimposed on the normal television picture. The circuitry operates as follows.

Data is fed into the level slicer 8 and is output to the clock generator 9. Initially the data for any line of any particular page of information to be displayed consists of synchronising bits to synchronise the clock generator 9. When this is completed the input data is scrutinised by the code and parity detect circuit 11 which detects, under the control of the program stored in the C.P.U. 13 the correct start code and the correct page number corresponding to the desired page number as determined by the user via the user control box 21. On detection of the desired page the information following is fed into the correct addresses in the random access memory 15 under the control via line 16 of the C.P.U. 13. As the data is fed into the random access

memory 15 it is monitored by the C.P.U. 13. Additional colour, flash or box signals are extracted from the data information and stored in the C.P.U. 13 for subsequent output to the control 20.

Information present in the random access memory may be called for by the C.P.U. 13 and changed, the altered information then being re-stored in the random access memory for subsequent display. The character generator 18 may be controlled by the C.P.U. 13 to produce a graphic or an alpha-numeric display.

Referring now to figure 2 one embodiment of the Central Processor Unit 13 is shown. The Central Processor Unit may for example be of the Intel 3000 series type. The C.P.U. 13 consists basically of a micro-program store 201 which has input and output connections to an Arithmetic and Logic Unit 202 which in turn has input and output connections to a control decoder circuit 203. The inputs to the control decoder circuit are as shown from the code and parity detect circuit on line 12, the clock on line 10 and the user control from control 21. The outputs of the control decoder are the Red (R) Green (G) and Blue (B) colour indicators, the flash indicator and the box indicator as described with reference to figure 1. Further outputs are the row number output (Row No.) the alpha/graphics output and the read/write instruction output to the random access memory 15 all shown symbolically as output line 16 in figure 1. Output line 16 also contains the address outputs to the Random Access Memory 15 from the Arithmetic and Logic Unit 202. The data bus 14 supplies information from the code and parity detect circuit 11 and from the Random Access Memory 15 to the Arithmetic and Logic Unit 202 and the information is transmitted from the Arithmetic and Logic Unit 202 to the Random Access Memory 15. Hence the data bus 14 may be considered, as marked in figure 1 bi-directional between the C.P.U. 13 and the R.A.M. 15 but only unidirectional between the code and parity detect circuit 11 and the C.P.U. 13.

The Arithmetic and Logic Unit (A.L.U. 202 consists of a number of electronic gates (e.g. AND, OR NAND NOR) and the operation of these gates is controlled by the micro-program store. The A.L.U. is therefore capable of performing a number of different functions (e.g. add/subtract/compare/inclusive OR). The micro-programme determines the sequence of events for the A.L.U. 202.

Some of the functions of the A.L.U. 202 are control functions the results of which are fed to the control decoder circuit 203 and other functions are merely to pass information received on data bus 14 straight on to

the R.A.M. 25.

Thus, for example, if the user selects a certain page the information is presented to the control decoder 203 and the A.L.U. 202 searches the incoming information for the required page number. Having detected the required page number the micro-programme receives a signal indicating this, and is stepped on to the next stage in the program.

The next stage may for example be the storage of any information subsequently appearing on the data bus in the required address positions in the R.A.M. 15.

The control decoder 203 also operates on information given out by the A.L.U. 202 and supplies information to the A.L.U. 202. Thus any colour information on input data bus 14 detected by the A.L.U. is stored in the control decoder for control of the display via control unit 20 (see figure 1).

In a preferred embodiment data information output from the code detect and parity block 11 is stored in the R.A.M. 15 and for example any colour information is ignored by the A.L.U. 202 and the control decoder 203. When the data is required for display the information in the R.A.M. 15 is fed under the control of the A.L.U. 202 to both the character generator 18 and to the A.L.U. 202. At this stage any colour etc. information is extracted and used to control the display via the control coder 203 and control box 20.

In a practical embodiment the output characteristics of control box 20 will be a function of the television set to which it is connected.

For the display of data transmitted for example over a telephone line the information is fed to data bus 14 and clocked into the random access memory 15 under the control of the central processing unit 13. The clock for the central processing unit and for the television display is generated internally within the central processing unit 13, energisation of this internal clock being by the user control 21 being operated to change the display system to display the information from the telephone line. In a similar manner data from a data modem may be stored in the random access memory 15 under the control of a clock within the data modem or a clock generated synchronously from the input data from the data modem. The display of the stored information however requires the generation of an internal high speed clock to provide the necessary television raster.

The program for each type of data will be different and normally only one such program will be provided per display system. It is

however possible to provide several programs in one or more micro program stores and to switch from one program to another under the control of the user control 21.

WHAT WE CLAIM IS:-

1. Receiving apparatus for a combined television/data display system in which information characterising data to be displayed is transmitted during line scan periods of a television signal when picture information is not being transmitted, comprising a memory for the storage of said information, character generator means for generating electric signals in respect of data characters to be displayed, and a central processing unit operable under the control of a program for controlling the storage of said information and the operation of said character generator means.

2. Receiving apparatus for a combined television/data display system as claimed in claim 1 wherein the central processing unit includes an arithmetic logic unit which is arranged to operate under the control of the program, a micro-program store for storage of the program and a control decoder, the arithmetic logic unit being connected for bi-directional transmission both to the micro-program store and to the control decoder and for reception of said information characterising data to be displayed.

3. Receiving apparatus for a combined television/data display system as claimed in claim 2 wherein said information is written into the memory under the control of addresses generated by the arithmetic logic unit.

4. Receiving apparatus for a combined television/data display system as claimed in claim 2 or claim 3 wherein the information characterising data to be displayed is signalled in specific line scan periods of a television signal, which specific line scan periods do not have picture information.

5. Receiving apparatus for a combined television/data display system as claimed in claim 4, including a clock generator synchronised to the received television signal, in which the control decoder of the central processing unit is connected to the clock generator for synchronisation of the central processing unit with the received television signal.

6. Receiving apparatus for a combined television/data display system substantially as described with reference to the drawings accompanying the provisional specification.

For the Applicants
J.D. DOLWIN
Chartered Patent Agent.

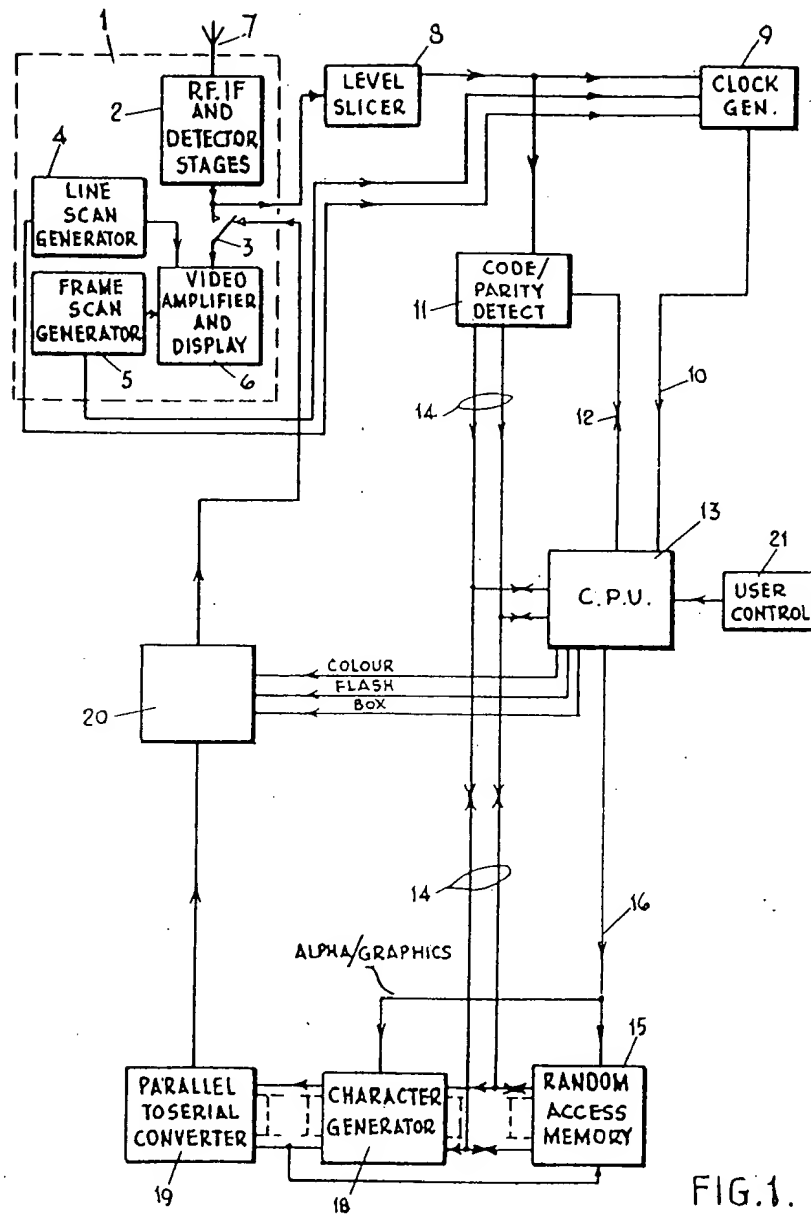


FIG. 1.

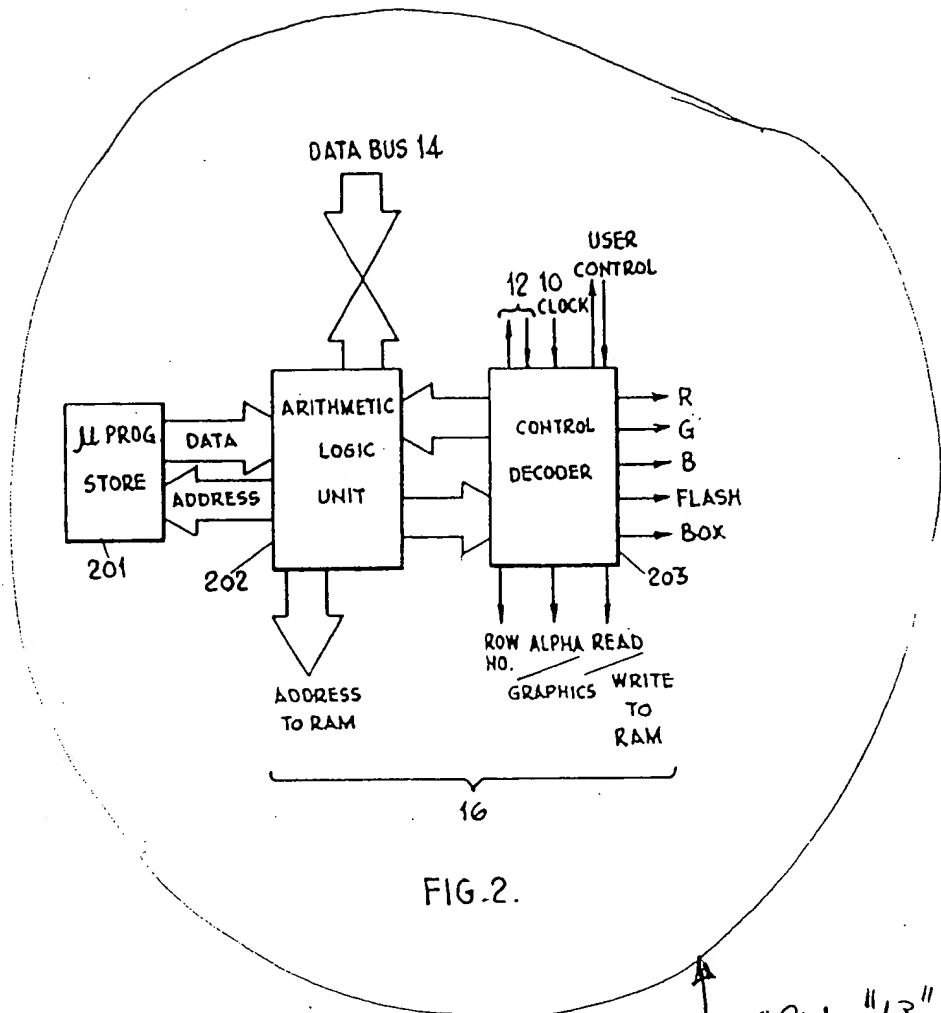


FIG. 2.

↑ CPU "13"
of figure 1